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AN10874

LFPAK MOSFET thermal design guide

Rev. 02 — 27 January 2011 **Application note**

Document information

Info	Content
Keywords	LFPAK, MOSFET, thermal analysis, design and performance, thermal considerations, thermal resistance, junction to ambient, junction to mounting base, thermal vias, JESD51, SMD, surface-mount, PCB design
Abstract	Thermal aspects are an important concern when designing for power MOSFETs. This is especially true for applications operating at higher ambient temperatures. This application note describes, in general terms, the different techniques which can be used during the design phase to ensure the PCB layout provides optimum thermal performance.

Revision history

Rev	Date	Description
02	20110127	final release
01	20091119	Initial version

Contact information

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1. Introduction

1.1 The need for thermal analysis

Power MOSFETs are commonplace in modern electronic circuit design, where they are frequently used to switch loads of many different types – ranging from a few milliamps or less to several tens of amps, depending on application. The popularity of power MOSFETs is almost certainly attributable to their ease of drive compared to their bipolar counterparts, together with the wide range of package, voltage and $R_{DS(on)}$ combinations which are now available.

Of course, MOSFETs are not perfect switches and neither are they indestructible, and the circuit designer should be aware of the following thermal considerations when designing a system employing MOSFET devices:

- Even when fully turned on, a MOSFET will dissipate power due to $I^2.R_{DS(on)}$ losses (where $R_{DS(on)}$ is the device on-state resistance)
- $I^2.R_{DS(on)}$ losses will result in temperature rises in the device and elsewhere
- MOSFETs may be damaged or destroyed by excessive device temperature

Thermal aspects are an important concern when designing with power MOSFETs, especially in applications which may be operating at elevated ambient temperatures, as the MOSFET junction temperature (T_j) must be kept below 175 °C if operation is to remain within specification. It is also important to bear in mind that the PCB to which the (surface-mount) MOSFETs are soldered will also have a maximum operating temperature of around 120 °C. The MOSFETs will be using the PCB as their primary method of heatsinking, and their dissipated heat energy will also cause PCB temperatures to rise. Care must therefore be taken that the PCB temperatures also remain within acceptable limits.

1.2 MOSFET R_{th} parameters and their limitations

In order to provide some measure of device thermal performance, it is normal industry practice for MOSFET data sheets to carry “thermal resistance” (R_{th}) figures. The concept of “thermal resistance” is analogous to that of electrical resistance, and is described in many texts on thermal management.

The two most common MOSFET thermal resistance values in data sheets are:

$R_{th(j\text{-}a)}$: The thermal resistance from device junction (die) to ambient. This is a single thermal resistance figure and is the net effect of all the possible series and parallel paths from junction to ambient. Typically this would include heat loss paths directly from the surface of the device package and also via the PCB to which the device is soldered

$R_{th(j\text{-}mb)}$: The thermal resistance from junction to mounting base. “Mounting base” is defined as the point at which the device would normally be soldered to a PCB, and is primarily a conduction path only.

The methods and conditions under which device thermal resistance figures should be measured are described in the JESD51-x series of standards, and as one might expect, the standards are very precise in their descriptions of how testing should be carried out. It might therefore be expected that the thermal resistance figures would be sufficient for a designer wishing to carry out thermal analysis of a system. Unfortunately, this is not the case, for the following reasons:

- $R_{th(j-a)}$ figures are highly dependent on PCB construction and layout, and the PCBs defined in the JESD51 standards are not generally representative of those found in real applications
- The PCBs specified by MOSFET manufacturers for their $R_{th(j-a)}$ data sheet figures almost never follow the JEDEC guidelines anyway, are often described in only the vaguest of terms and are inconsistent from manufacturer to manufacturer
- The $R_{th(j-a)}$ test methods do not allow for several devices mounted in close proximity on the same PCB (a typical arrangement in a real-life application)
- Thermal resistance $R_{th(j-mb)}$ is only one part of the total thermal pathway from junction to ambient

Clearly then, the thermal resistance figures $R_{th(j-mb)}$ and $R_{th(j-a)}$ as published are of little practical use in the thermal analysis of real-life circuits and systems. In fairness to JEDEC, R_{th} figures were never intended to be used for design or system analysis, as this note from *specification JESD51-2* indicates:

"…The purpose of this document is to outline the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient ($R_{th(j-a)}$) thermal resistance measurement in natural convection. The intent of ($R_{th(j-a)}$) measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment."

Sadly, despite this clear statement from JEDEC, we still see many instances of designers attempting to use data sheet R_{th} figures in thermal design and analysis exercises.

1.3 Aim of this document

Having determined that the data sheet R_{th} figures are not appropriate for carrying out thermal analysis of real-life applications, it is natural to ask: what is the alternative? Unfortunately there is no simple method of thermal analysis which is applicable to complex situations whilst offering a reasonable degree of accuracy. The heat transfer mechanisms involved are simply too complex with too many interacting thermal pathways to allow for a simple yet valid method of analysis. In general, such analysis may only be carried out by either:

- recreating the scenario in simulation using computer-based simulation

or

- building the scenario in real-life and performing an experimental evaluation

The former approach can yield accurate, rapid results at the cost of expensive software and the necessary skills required to operate it, whilst the latter incurs the time and cost associated with building and measuring a representative model.

We recognize that a third approach may also be of use, particularly in the early stages of PCB design, which bridges the gulf between the less-than-helpful R_{th} figures at one extreme and full prototype simulation or build at the other. This document will illustrate, in general terms, the different techniques which may be applied to typical PCB design, in order to steer the layout towards one which has optimum thermal performance. Factors which will be considered include:

- PCB layer stack-up
- The influence of common circuit topologies on PCB layout
- PCB copper area
- The influence of thermal vias
- Device placement and spacing
- The implications of multiple dissipating devices on a single PCB

This document cannot hope to address all the myriad possible combinations of device placement, layer stack-up and so forth. Rather, its intention is to provide initial guidance to the engineer who, faced with a brand new design task, and a lack of helpful information, may be asking himself; “How can I be sure my devices will run at safe temperatures?”

Finally, it almost goes without saying that the information contained within this design guide is presented as a starting point only. Any new design should of course be prototyped and its thermal behavior characterized before placing the design into production.

2. General approach to thermal analysis

2.1 The use of thermal simulation software

In order to allow fast and flexible analysis of multiple parameter variations, the thermal analyses presented in this document have been carried out using thermal simulation software. The simulations use MOSFET models which have been validated against empirical data and are known to accurately model the thermal behavior of real-life devices.

The thermal simulation software used to carry out the analyses is the Mentor Graphics (Flomerics) “Flotherm” package. The device models used in the analysis are available for free download from the NXP Semiconductors website.

2.2 Simulation set-up

The PCBs to be considered have the following general characteristics:

- They are surface-mount designs and the MOSFETs are in the surface-mount LFPAK packages
- PCB stack-ups range from 1 to 4-layer construction, but always have an overall thickness of 1.6 mm
- PCB material is standard FR4, with a rated maximum operating temperature of 120 °C
- Copper thickness on all layers is 1 oz./ft^2 (35 μm)
- The PCB is suspended in free air

Other important factors:

- The ambient temperature is 20 °C
- The simulations solve for conduction, convection and radiation heat transfer
- MOSFET power dissipation is 0.5 W per device
- There is no forced air cooling applied i.e. only natural convection is modeled

2.3 PCB layout and stack-up

2.3.1 Factors influencing, PCB layout and stack-up

When laying out a PCB we do not have a completely free choice as to where we can place the MOSFET devices and other components and how we connect them together. Usually, device placement and connection is a question of reconciling various (often conflicting) requirements. The factors influencing component placement may include:

- Circuit topology
- Design for ElectroMagnetic Compatibility (EMC)
- Design for thermal performance
- The necessity to situate certain components (e.g. connectors) in pre-defined locations
- The need to provide low-resistance and low-inductance current paths in specific areas

If we are considering a PCB design from a thermal perspective, then the ideal thermal design may have to be compromised in some respects in order to accommodate the other requirements placed on the design.

2.3.2 Circuit topology

Circuit topology is perhaps the least flexible of all the factors influencing PCB design. After all, if the components are not connected together in the proper manner then the circuit will not function as expected. The topology will also dictate which MOSFET terminals may be connected to copper planes and hence may use those planes to help dissipate heat energy. This is particularly important for a surface-mount package such as LFPAK, where the primary thermal pathway out of the package is through the device drain tab on the underside of the device. Circuit topology therefore has a very great influence on the thermal design and consequent device operating temperatures.

Several different topologies will be considered in this guide, and it is believed that these will be relevant to a large number of typical end-user applications.

2.3.3 Design for ElectroMagnetic Compatibility (EMC)

The subject of design for electromagnetic compatibility is a complex one and is well beyond the scope of this document. However, one of the simpler aspects of design for EMC is highly relevant to thermal design - the provision of a ground plane layer in the PCB.

From an EMC perspective, a multilayer PCB should have at least one copper layer which is used exclusively as a ground plane, and which has a minimum of holes and breaks in it. This requirement is not in conflict with good thermal design - indeed, the presence of a continuous layer of copper in the PCB stack-up can only enhance the thermal performance of the board as a whole. PCB layouts which incorporate a dedicated ground plane will be considered in all of the following analyses.

3. A single LFPAK device

This section will examine the factors influencing the thermal performance of a single LFPAK device on PCBs of several different configurations. From this point onward the phrase “thermal performance” is used when discussing the ability of a stack-up or structure to remove heat energy from the device(s). In order to build up a comprehensive picture of the factors influencing thermal performance, we will begin with the simplest 1-layer stack-up and then systematically add additional layers to the PCB.

3.1 Analysis 1: A single-layer PCB

The simplest possible PCB stack-up is that of a single top copper layer; a 1-layer stack-up. In analysis 1 we will examine the variation in device junction temperature (T_j) as a function of top copper area. See Figure 1.

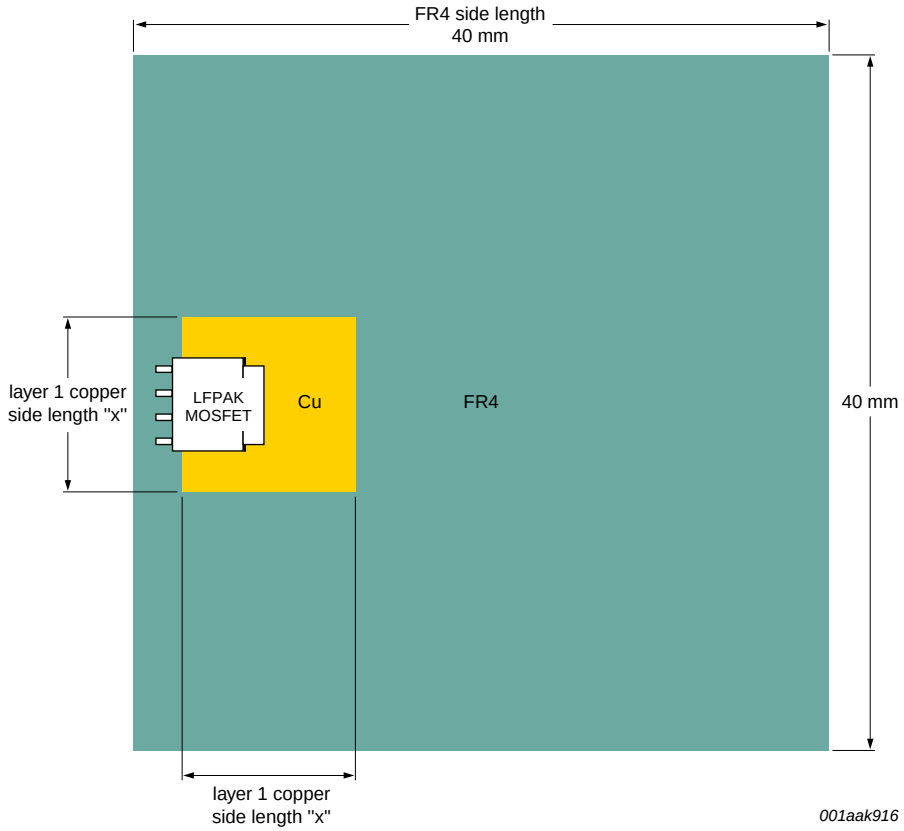
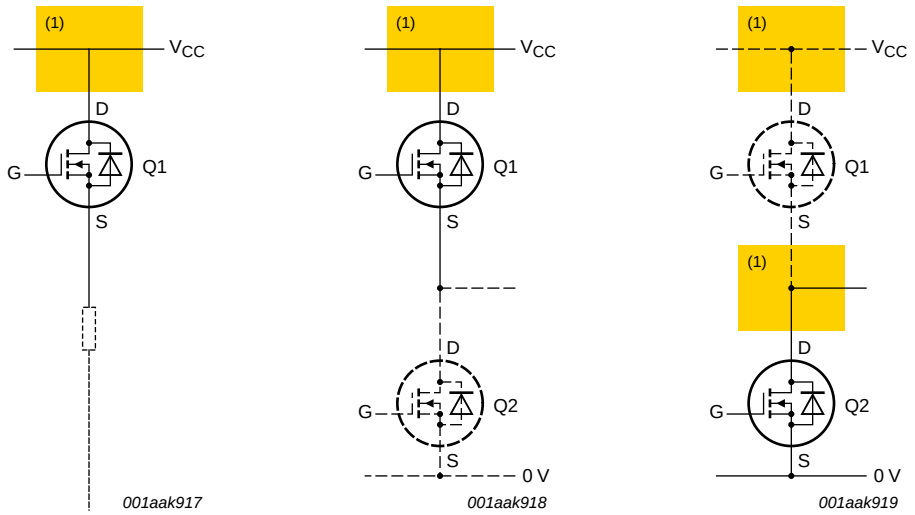


Fig 1. Single device; 1-layer stack-up

Figure 1 illustrates the MOSFET device mounted on a square area of layer 1 copper of side length “x” and with FR4 of size 40 mm × 40 mm. Three possible circuit configurations corresponding to this layout are shown in Figure 2.



(1) Plane available for cooling

a. High-side load switch set-up: MOSFET Q1

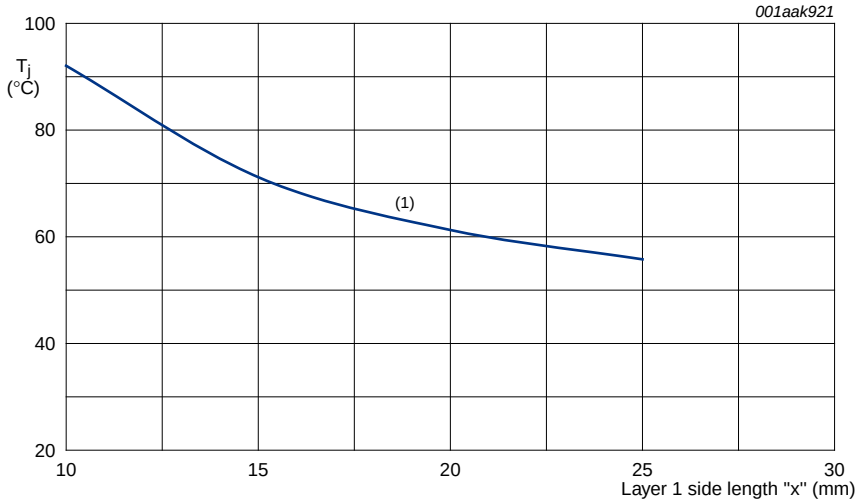
b. Half-bridge set-up: MOSFET Q1 and Q2

c. Half-bridge set-up: MOSFET Q2 and Q1

Fig 2. Three possible circuit configurations for the layout of Figure 1

Figure 2(a) shows MOSFET Q1 configured as a high-side load switch, with its drain tab connected to the V_{CC} plane (in yellow). Figure 2(b) and Figure 2(c) demonstrate MOSFETs Q1 and Q2 connected in a half-bridge configuration. Again, both devices are primarily cooled by planes connected to their drain tabs, although for Q2 the plane corresponds to the mid-point of the half-bridge rather than a power plane. A small degree of additional cooling may also be realized by attaching planes to the MOSFET sources, although the source pins are not the primary heat path out of the package and so the additional benefit is minimal. Generally speaking, the primary heat path is through the package drain tab and into whatever plane is attached to this connection, and it is this configuration which will be considered in this guide.

By carrying out simulations for several sizes of “x” we can determine how the device junction temperature (T_j) varies with copper area. The results are shown in Figure 3. Remember that the ambient temperature is 20 °C.



(1) Layer 1 only.

Fig 3. Device junction temperature versus layer 1 top copper side length "x"

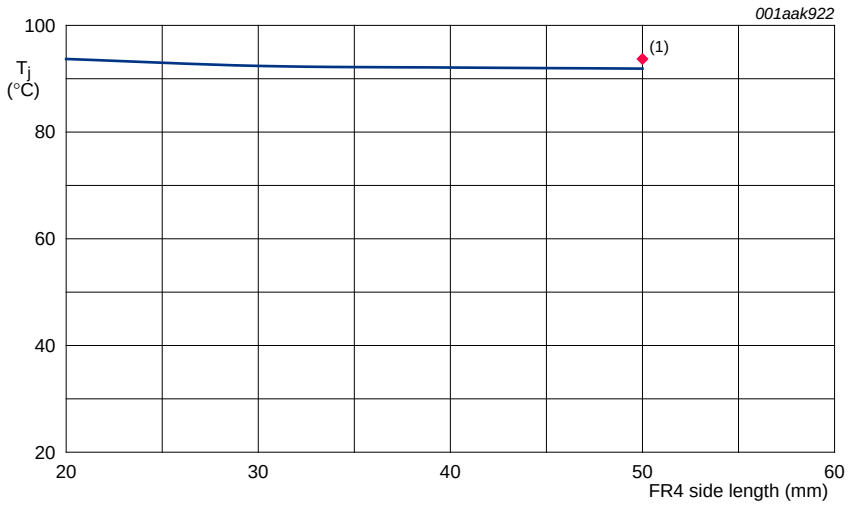
The graph of Figure 3 has two notable features:

- T_j depends greatly on side length “x” and hence layer 1 copper area
- The ability of the top copper to provide heatsinking for the MOSFET displays the “law of diminishing returns”. In other words, we cannot keep adding more copper area to layer 1 in the hope of continuing to reduce T_j. Rather, from the shape of the curve we might conclude that T_j will never decrease below, say 50 °C no matter how much copper area we provide on layer 1

Section 1.1 1 it was stated that there are in fact two limiting temperatures which must not be exceeded - MOSFET T_j and the temperature of the PCB material T_{PCB}. For surface-mount MOSFETs, the point of maximum T_{PCB} will usually occur under the centre of the MOSFET tab, as one might expect. For MOSFETs in the LFPAK package, T_{PCB} will typically track T_j to within less than 0.5 °C, and therefore we can reasonably say that $T_{PCB} \approx T_j$. This assumption will be made for the remainder of the analyses of the LFPAK package. The results of Figure 3 therefore indicate that, for a PCB whose T_{PCB} (max) is 120 °C, we should not encounter problems with PCB degradation for even the smaller areas of layer 1 copper area, provided that the ambient temperature stays below approximately 45 °C.

3.1.1 The role of FR4 size in analysis 1

The choice of FR4 PCB area in Section 3.1 may seem both arbitrary and unrepresentative of the PCB size in a real-life application. In this section, however, we will see that the area of bare FR4 has almost no influence on device (T_j). To demonstrate this principle, additional simulations were carried out with FR4 dimensions of 20 mm × 20 mm, 30 mm × 30 mm, 50 mm × 50 mm, with the layer 1 copper area fixed at 10 mm × 10 mm. The results are shown in Figure 4.



(1) With additional layer 1 copper shown.

Fig 4. Junction temperature versus FR4 side length

The results of Figure 4 demonstrate that the size of bare FR4 has almost no impact on device T_j. This is in marked contrast to the results of Figure 3 where we varied the layer 1 copper area. The difference between the two sets of results is easily understood when we compare the thermal conductivities of copper and FR4; copper has a thermal conductivity of around 380 W/(m.K) whilst for FR4 the figure is only around 0.6 W/(m.K). As thermal conductivity is a measure of how easily heat energy travels through a substance, it should be clear that adding even a large area of FR4 (which is a poor conductor) is nowhere near as effective as adding a much smaller area of highly conductive copper

We can further illustrate the insulating properties of FR4 by adding some unconnected areas of layer 1 copper to the model, as shown in Figure 5.

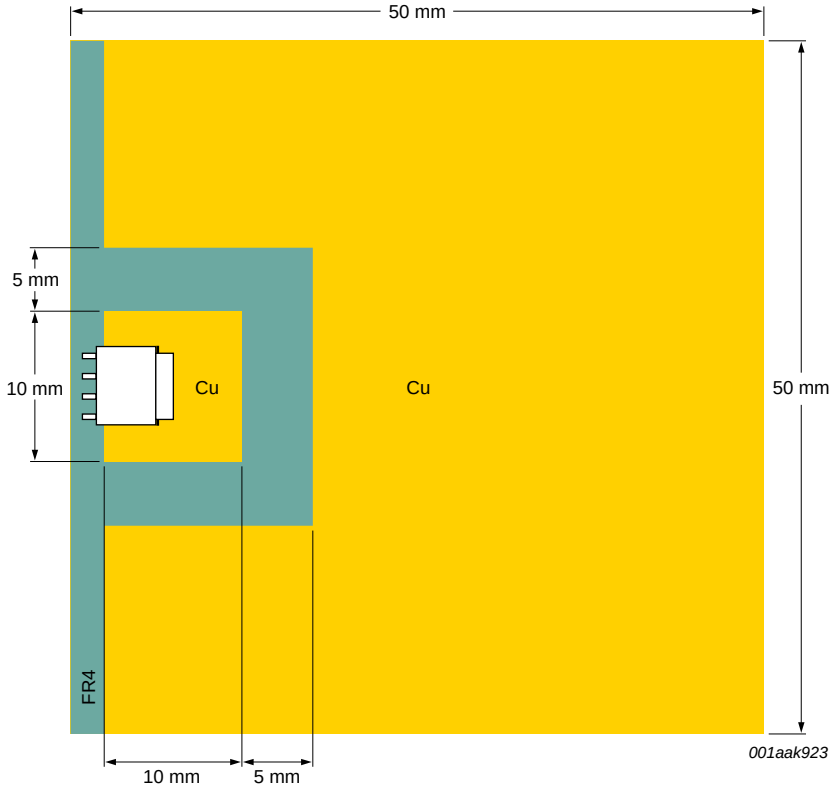
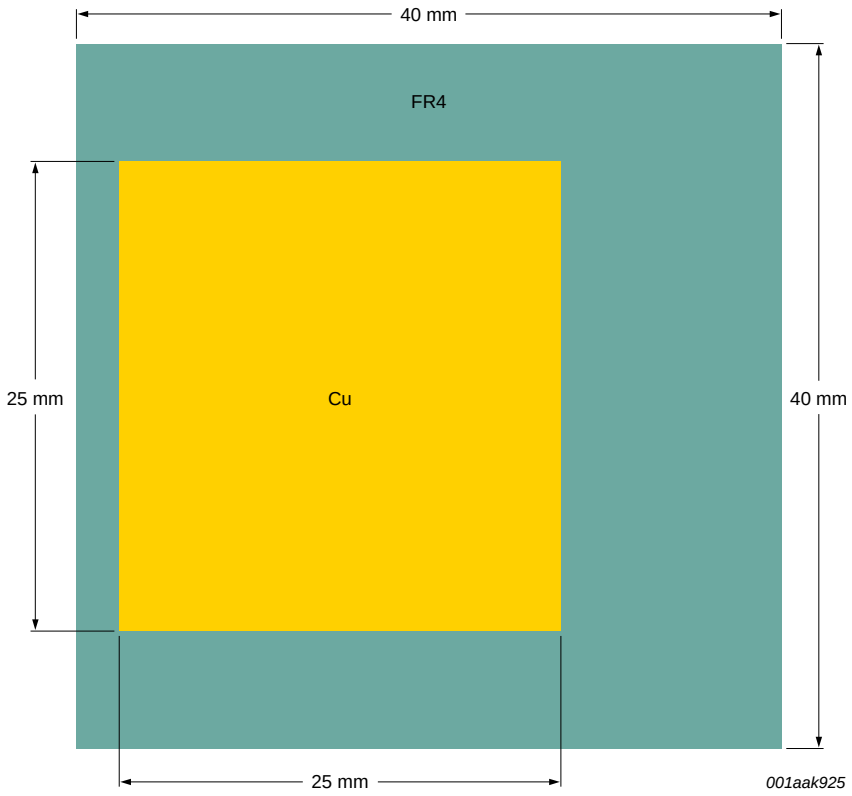


Fig 5. Adding additional layer 1 copper to the 50 mm × 50 mm FR4 board

Figure 5 shows the 50 mm × 50 mm FR4 layout with most of the layer 1 area filled with a "flood" of copper. A gap of 5 mm has been left around the device and its attached 10 mm × 10 mm copper area. Although we might have expected the additional layer 1 copper to make a significant difference to device T_j, in fact this is not the case. The heat energy is prevented from utilizing the additional "heatsinking" area by the isolation gap around the device and the poor thermal conductivity of the intervening FR4. The ability of FR4 to "thermally isolate" heat sources in this way is important and will be demonstrated again in Section 4 "Two LFPAK devices" on page 19 and Section 5 "Four LFPAK devices" on page 29.

3.2 Analysis 2: 2-layer PCB

For the purposes of this exercise we will again consider the same variations in layer 1 copper as for analysis 1. However for analysis 2 we will add the layer 4 (bottom copper) layer measuring a fixed 25 mm × 25 mm, thereby creating a 2-layer stack-up. The bottom copper layer is shown in Figure 6.

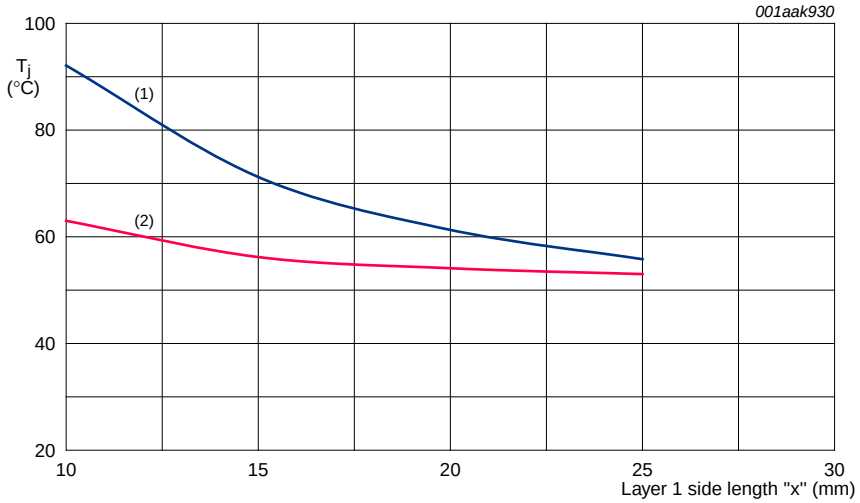


The PCB is viewed from below.

Fig 6. Layer 4 copper

In practical terms this layer might be a ground or power plane, although the device is not electrically connected to this layer.

As with analysis 1 (Section 3.1 on page 7), we can again carry out simulations for various layer 1 side length “x”, keeping the size of the layer 4 plane constant at 25 mm × 25 mm. The results are shown in Figure 7, together with those from analysis 1 for comparison purposes.



(1) Layer 1 only.

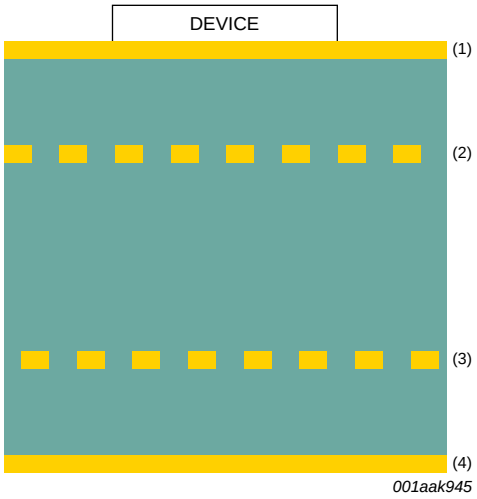
(2) 2-layer.

Fig 7. Device junction temperature versus layer 1 copper side length “x” for the 1 and 2-layer PCB stack-ups

Figure 7 demonstrates that adding the layer 4 copper has significantly improved the thermal performance of the PCB, even though layer 4 is not directly connected to the MOSFET. We can also see that the MOSFET T_j is now somewhat less dependent on layer 1 copper area. By adding the second layer we can reduce the top copper side length from 25 mm × 25 mm to approximately 15 mm × 15 mm whilst retaining the same thermal performance (i.e. the same device T_j). This is certainly a useful result if we wish to increase component density on layer 1!

3.3 Analysis 3: A 4-layer PCB part 1

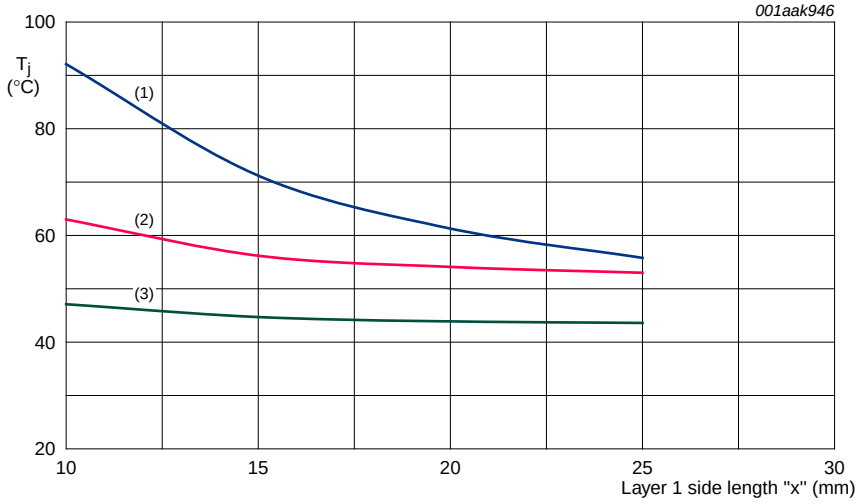
This document will consider several different variations of the 4-layer PCB stack-up. The simplest of these variations is based on the 2-layer stack-up of analysis 2 (Section 3.2), with the addition of two additional internal signal layers. It is assumed that the additional layers would be mainly composed of many thinner signal tracks, rather than large continuous planes. Detailed simulation of these layers is obviously not feasible, and so a “percentage coverage” method is adopted instead. With this method, the average conductivity of the structure is calculated based on the percentage of total area covered in copper and the layer thicknesses. For the purposes of these exercises, we will assume that the signal layers have 50 % copper coverage and are also of 1 oz./ft^2 (35 μm) thickness. The 4-layer structure is summarized in Figure 8.



(1) Layer 1, 35 μm, variable area.
(2) Layer 2, 35 μm, 50 % coverage.
(3) Layer 3, 35 μm, 50 % coverage.
(4) Layer 4, 35 μm, 25 mm × 25 mm.

Fig 8. 4-layer stack-up for analysis 3, part 1 (not to scale)

As before, we will carry out simulations for various sizes of layer 1 copper, keeping the other layers constant. The results are shown in Figure 9 together with those from the previous two analyses. Note that there is again no direct connection between the MOSFET and layer 4 plane, and the corresponding circuit topologies would be those shown in Figure 2 on page 8



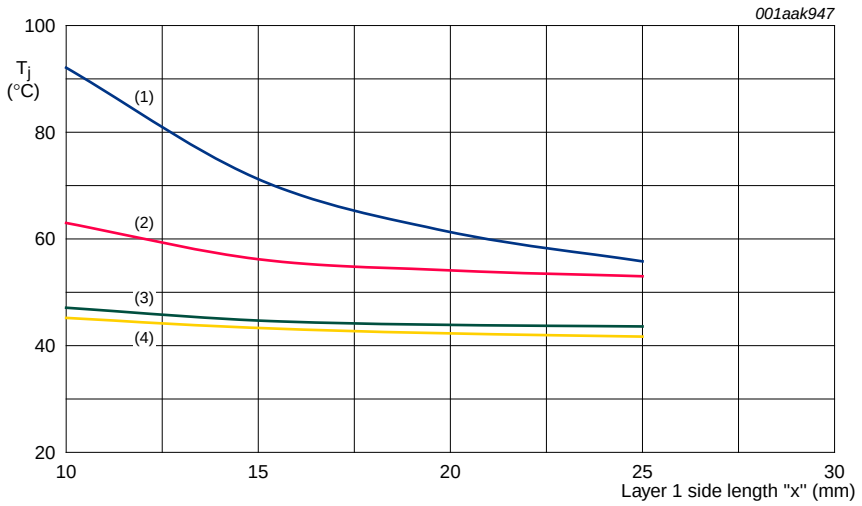
(1) Layer 1 only.
(2) 2-layer.
(3) 4-layer.

Fig 9. Device junction temperature versus layer 1 copper side length “x” for the 1, 2 and 4-layer PCB stack-ups

Adding copper layers 2 and 3 to the design has resulted in a considerable reduction in T_j compared to the 1 and 2-layer stack-ups. In addition, it can be seen that T_j has become almost independent of layer 1 copper area. This is a useful result which indicates that, in a 4-layer PCB stack-up similar to that described here, we can reduce the layer 1 copper area to a minimum without drastically compromising the thermal performance of the design. The layer 1 copper area which has been freed up may therefore be used for mounting other devices, routing tracks, and so on.

3.4 Analysis 3: A 4-layer PCB part 2

The second 4-layer stack-up which will be considered is similar to that of Figure 8, except that layer 2 has been replaced with a plane of 100 % area coverage. This might represent an internal ground plane. Otherwise, the analysis is the same as that for part 2. The results are shown in Figure 10.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer (layer 2 100 % coverage).

Fig 10. Device junction temperature versus layer 1 copper side length “x” for the 1, 2 and 4-layer PCB stack-ups, and for the 4-layer stack-up with layer 2 area coverage of 100 %

It is interesting to see that increasing the percentage coverage of layer 2 from 50 % to 100 % has yielded little improvement in thermal performance. In other words, an internal plane is less effective than an external plane in terms of reducing device temperature. This can be explained by understanding that an external plane is able to lose heat energy to the external environment by convection and radiation loss from its surface. An internal layer, however, is obviously not exposed to free air (except, perhaps, for a negligible amount at the plane’s edges) and so the only contribution it makes to improved cooling is to increase the through-board conductivity of the PCB.

3.5 Analysis 4: A 4-layer PCB with thermal vias part 1

So far we have considered cases where the layer 1 copper (connected to MOSFET drain) has not been connected to any other layer. However, it is entirely possible that we would use a pattern of vias under the MOSFET tab to provide electrical connection with a V_{CC} plane on layer 4 (for instance). This approach is consistent with the topologies of Figure 2. As well as providing the necessary electrical connectivity, this arrangement will also provide an additional thermal pathway away from the MOSFET, whereby the “electrical vias” also function as “thermal vias”.

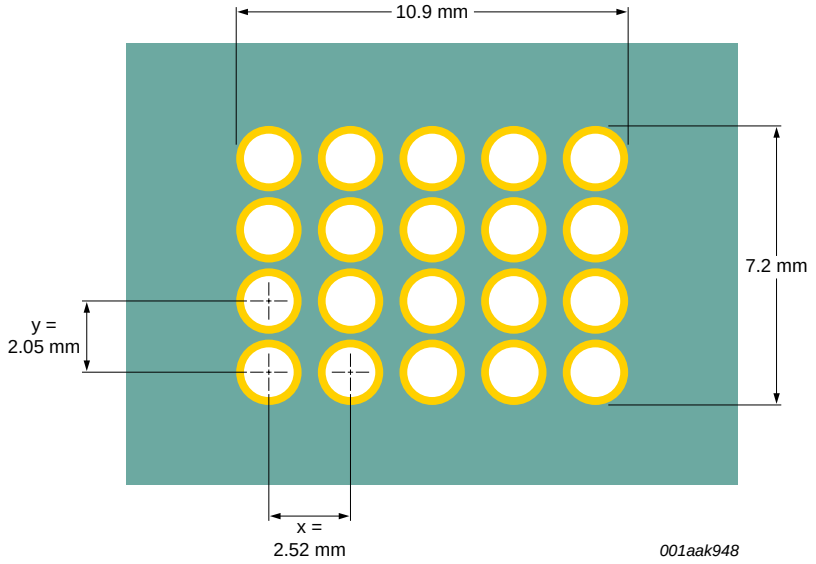
Whilst it is known that in general terms adding vias under a device will improve its thermal performance, it can be difficult to know how many vias provide an optimal solution. Obviously we do not want to add too many vias if they do not significantly improve thermal performance, as their presence may cause problems during PCB assembly (and, of course, we are paying for every via on the PCB!). The purpose of this analysis is therefore to examine the impact of various via patterns on the thermal performance of the design.

The analysis in this section will use a layer 1 copper area of side length 15 mm and will consider via patterns with the characteristics listed in Table 1. In all cases, vias are 0.8 mm diameter and are assumed to be air-cored. PCB stack-up is as Figure 8. An example via pattern is shown in Figure 11.

Table 1. Via patterns summarised

Number of vias			Via pitch x (mm)	Via pitch y (mm)	Overall via pattern dimensions (mm × mm)
Total	x	y			
0	0	0	-	-	-
20[1]	5	4	2.52	2.05	10.9 × 7.2
30	5	6	2.52	1.33	10.9 × 7.5
54	9	6	1.26	1.26	10.9 × 7.1
63	9	7	1.26	1.26	10.9 × 8.4
77	11	7	1.04	1.04	11.2 × 7.1

[1] See Figure 11.



Drawing not to scale.

Fig 11. The 5 × 4 via pattern

The results for the different via patterns are shown in Figure 12.

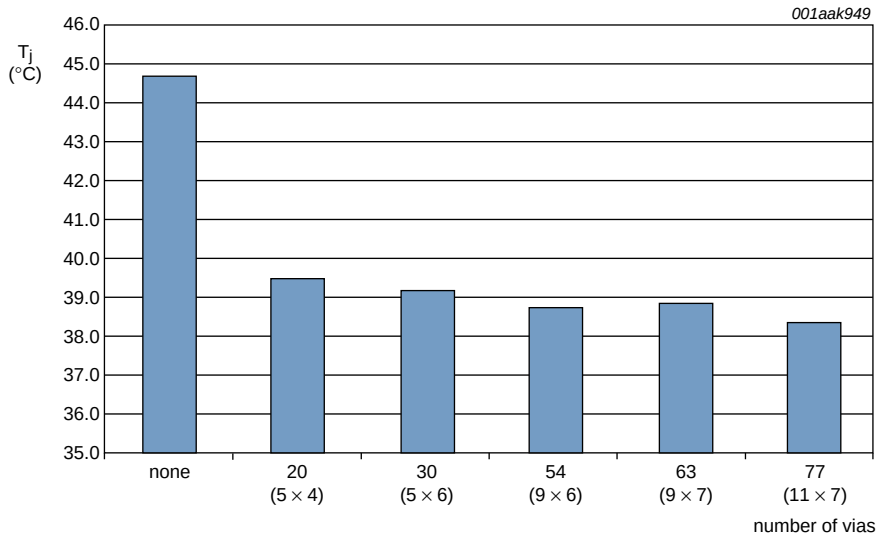


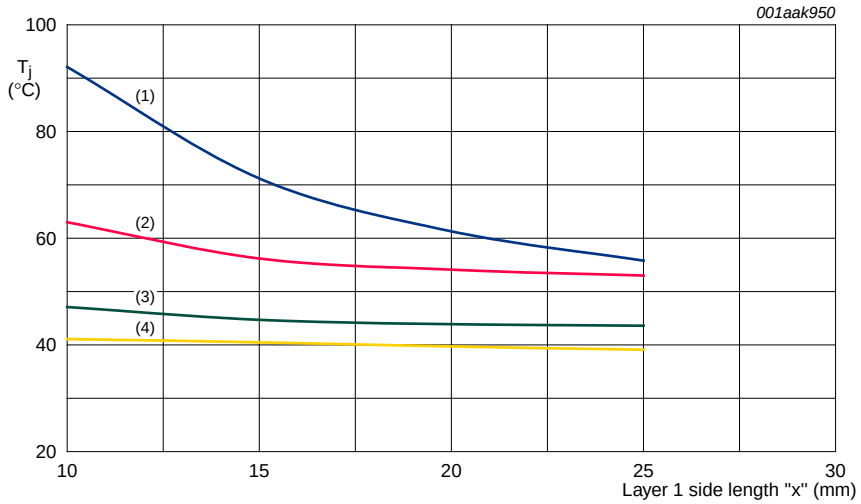
Fig 12. Device junction temperature versus the number of vias

Figure 12 demonstrates a notable decrease in device T_j when moving from a situation with no vias under the device to one of 20 vias under the device. This is a clear indicator that the heat energy is being conducted from the MOSFET drain tab to layer 4 and is exactly the result we would expect. It is interesting to note, though, that adding progressively more vias under the device results in little additional decrease in T_j. This is because, as we add more vias, so the through-board conductivity of the layout increases. However, at the same time we are also decreasing the area of contact between device and PCB as more layer 1 copper is replaced with air. Consequently we do not see much

improvement in thermal performance. The conclusion we can therefore draw from this exercise is that adding some vias will improve thermal performance, but continuing to add more vias will not yield further significant performance improvements.

3.6 Analysis 4: A 4-layer PCB with thermal vias part 2

For completeness, the “4-layer plus vias” structure has also been simulated for several sizes of layer 1 copper, with the stack-up again as Figure 8 on page 14. The results are shown in Figure 13.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer; 5 × 4 vias.

Fig 13. Device junction temperature versus layer 1 copper side length “x” for the 1, 2 and 4-layer PCB stack-ups and for the 4-layer stack-up with vias

It can be seen that, once vias are added under the device, T_j becomes almost independent of top copper area, and is approximately 5 °C lower than for the 4-layer stack-up without vias.

3.7 Summary: factors affecting the thermal performance of a single device

- For a device mounted on a 1-layer PCB, device T_j depends heavily on copper area. However, the “law of diminishing returns” applies and simply adding more and more layer 1 copper does not yield commensurate improvements in thermal performance (see Figure 3). The lowest achievable T_j, with a large copper area, would be approximately 50 °C.
- Varying the size of the PCB FR4 does not significantly influence device T_j if the copper connected to drain is kept at a constant size. Similarly, adding unconnected copper areas onto an extended FR4 area also does not significantly influences T_j (see Figure 4).

- Adding a second copper layer (layer 4) provides a significant improvement in thermal performance and reduces the dependence of T_j on layer 1 copper area (see Figure 7).
- Moving to a 4-layer PCB stack-up again provides a significant improvement in thermal performance compared to 1- and 2-layer stack-ups. In addition, the dependence of T_j on layer 1 copper area is further reduced (see Figure 9 and Figure 10).
- Adding vias under the device provides a further improvement in thermal performance, but once again the law of diminishing returns applies, whereby adding more and more vias yields little significant benefit (see Figure 12).
- With vias under the device, the dependence of T_j on layer 1 copper area is almost eliminated (see Figure 13).

The single device configuration with 15 mm × 15 mm top copper and 20 vias will be used as a building block in the analyses presented in the following sections (Section 4.1 on page 20 to Section 5.4 on page 32).

4. Two LFPAK devices

Section 3 considered the thermal performance of a single device mounted on a section of PCB. The next level of complexity in this analysis is that of two devices mounted on a PCB, where we will observe the effect of device separation on T_j. In order to restrict the number of variables to a sensible limit we will consider only the 15 mm × 15 mm side-length area for layer 1. However, the PCB size has been increased to 120 mm × 80 mm to allow more scope for investigating different device separation distances. As before, we will begin with the simple 1-layer stack-up and then progressively add layers to the board.

The PCB top copper configuration is shown in Figure 14.

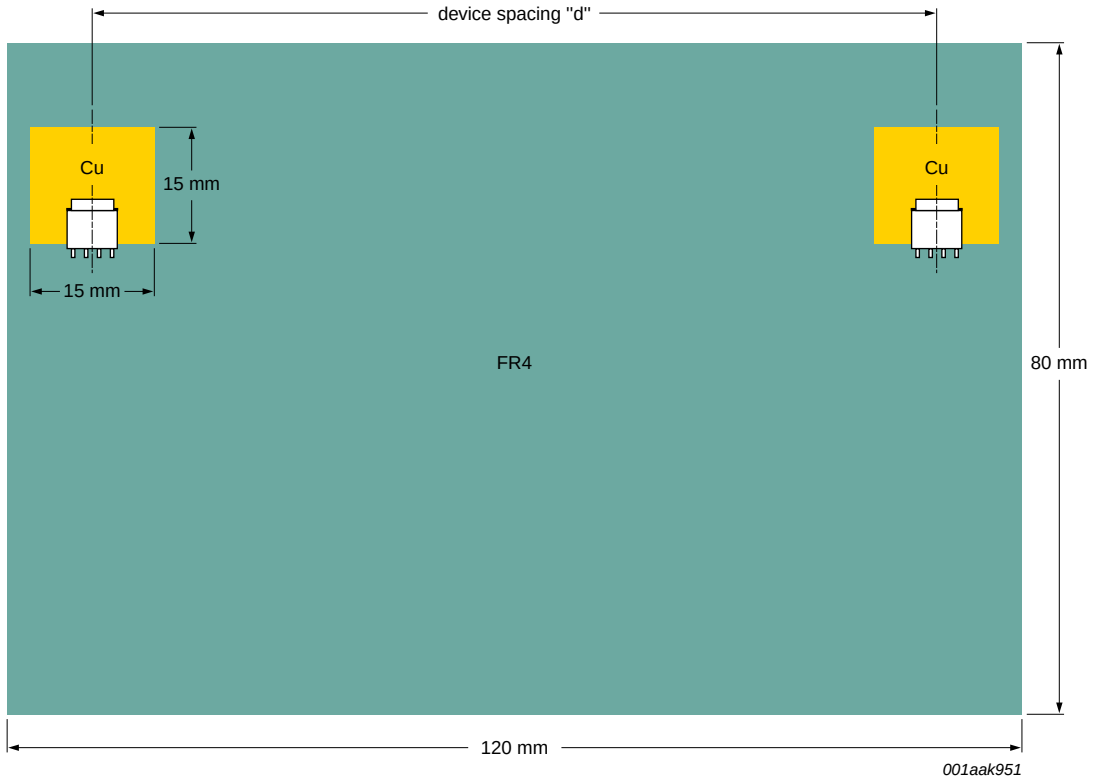
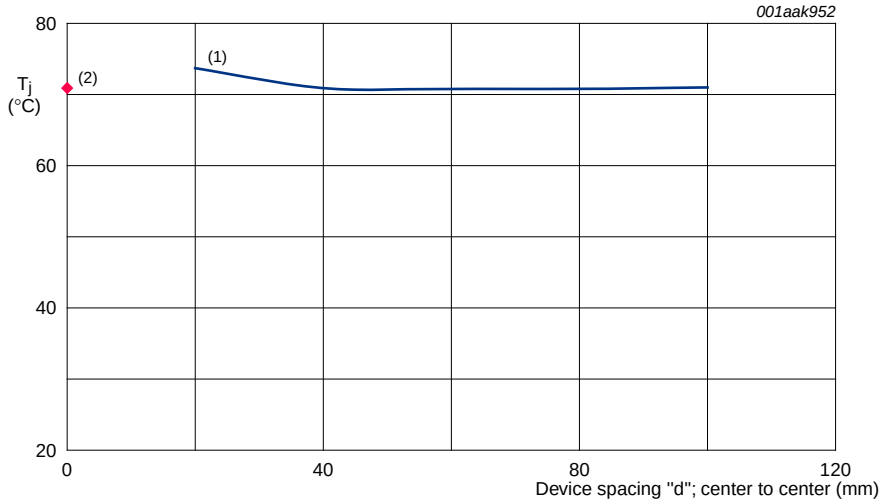


Fig 14. PCB top copper configuration for the analysis of two devices

Simulation were carried out to investigate the influence of “d” on device T_j for the various PCB stack-ups. Values of d varied from 100 mm (maximum separation, devices mounted near the PCB edges, as shown in Figure 14) to 20 mm, where there was only a 5 mm gap between the device layer 1 copper areas value.

4.1 Analysis 5: A single-layer PCB

The results for the single-layer simulations are shown in Figure 15. As the placement of the devices is symmetrical about the board centre line, regardless of d, the thermal performance of both devices is almost identical and so the T_j figure may be taken to be for either device. T_j for a single device, mounted near the PCB edge, is also shown.



(1) Layer 1 only.

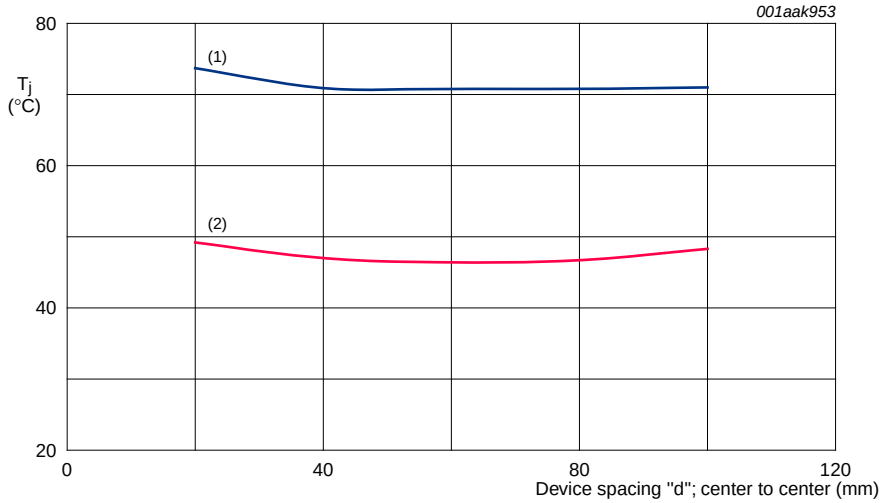
(2) Single device.

Fig 15. Simulation results for two devices of varying separation “d” on a single-layer PCB. The result for a single device mounted at the PCB edge is also shown

Even though the two devices are mounted on the same PCB, it is interesting to note that they perform as almost completely independent units – T_j is largely the same as for the single device and is not unduly influenced by device separation except for the case where the devices are mounted closest together (“d” at a minimum). This is a consequence of the poor thermal conductivity of the FR4 PCB material which effectively “isolates” the two devices in most cases, as discussed in Section 3.1.1 on page 9.

4.2 Analysis 6: A 2-layer PCB

For the purposes of this exercise we will again consider the same variations in device spacing as for analysis 5 (see Section 4.1). However for analysis 6 we will add the layer 4 (bottom copper) layer covering the whole of the underside of the PCB and thereby creating a 2-layer stack-up. In practical terms this layer might be a ground or power plane, although as far as the board thermal performance is concerned it makes no difference as the devices are not connected to this layer. The results are shown in the graph of Figure 16 together with those from analysis 5 for comparison purposes.



(1) Layer 1 only.

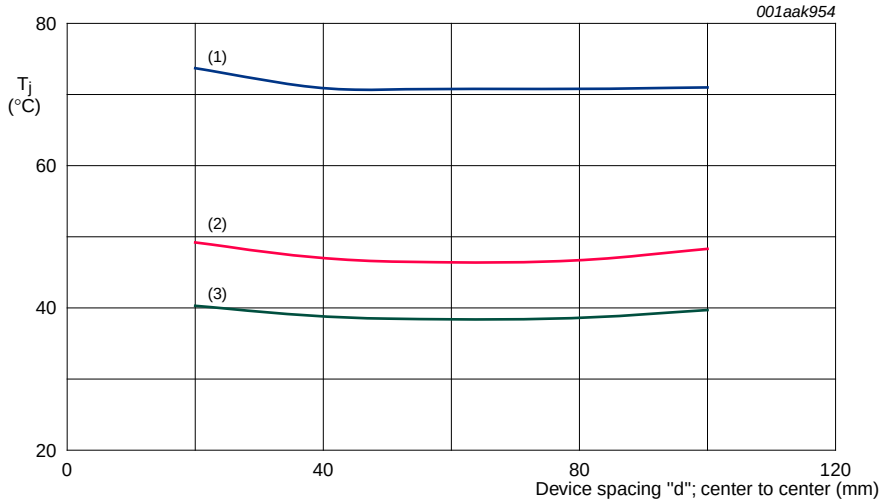
(2) 2-layer.

Fig 16. Simulation results for two devices of varying separation “d” on a 2-layer PCB

Adding the second copper layer has considerably reduced the junction temperatures of both devices, as one might expect, and temperature still remains largely independent of device separation.

4.3 Analysis 7: A generalized 4-layer PCB

The 2-layer stack-up of analysis 6 will now be increased to 4 layers with the addition of two internal signal layers. As before, it is assumed that these layers would be mainly composed of many thinner signal tracks, rather than large continuous planes. Simulation of the internal layers will again be by the “percentage coverage” method, with the assumption of 50 % copper coverage and 1 oz./ft^2 (35 μm) thickness. Layer 4 remains unconnected to either device, also as before. The 4-layer structure is therefore as summarized in Figure 8. Layer 4 remains a solid plane covering the entire underside area and junction temperatures are determined for various separation distances “d”. The results are shown in Figure 17.



(1) Layer 1 only.

(2) 2-layer.

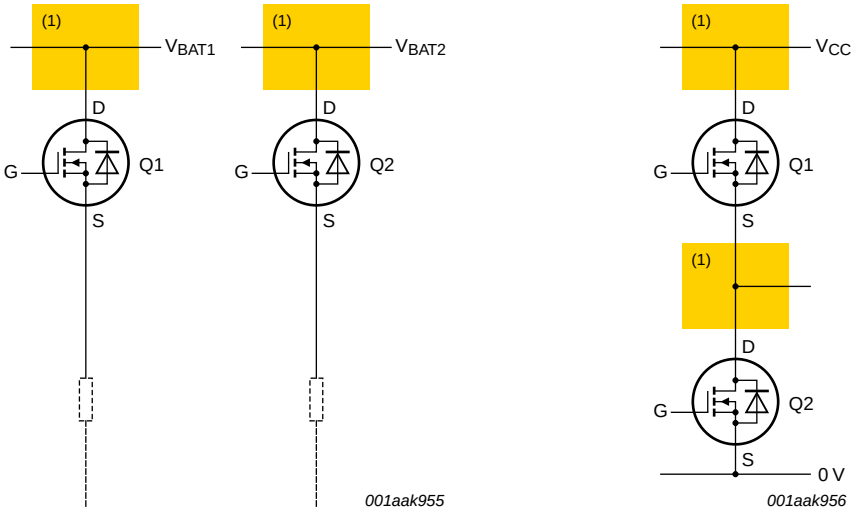
(3) 4-layer.

Fig 17. Simulation results for two devices of varying separation “d” on a 4-layer PCB

The addition of the two internal layers results in curve of similar shape to the 2-layer stack-up but with an overall reduction in T_j of approximately 10 °C.

4.4 Analysis 8: A 4-layer PCB with thermal vias part 1

In analyses 8 and 9 we will consider cases where the layer 1 copper (connected to MOSFET drains) is connected to layer 4 by thermal/electrical vias of the 5 × 4 via pattern described in Section 3.6. The layer 4 copper area will be reduced to two 15 mm × 15 mm planes, with a plane connected to each MOSFET. When using vias to connect one or more layers together for thermal reasons, we must also consider the implications for circuit topology and layer stack-up. For the configuration examined in this section, the possible circuit topologies are shown in Figure 18.



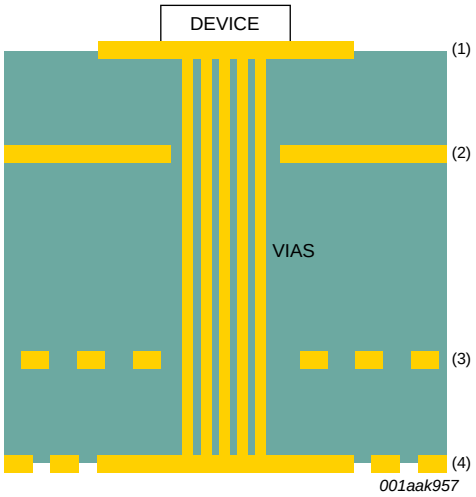
(1) Plane available for cooling

a. High-side load switches

b. Half bridge configuration

Fig 18. Possible circuit configurations for two MOSFETs with independently connected drains

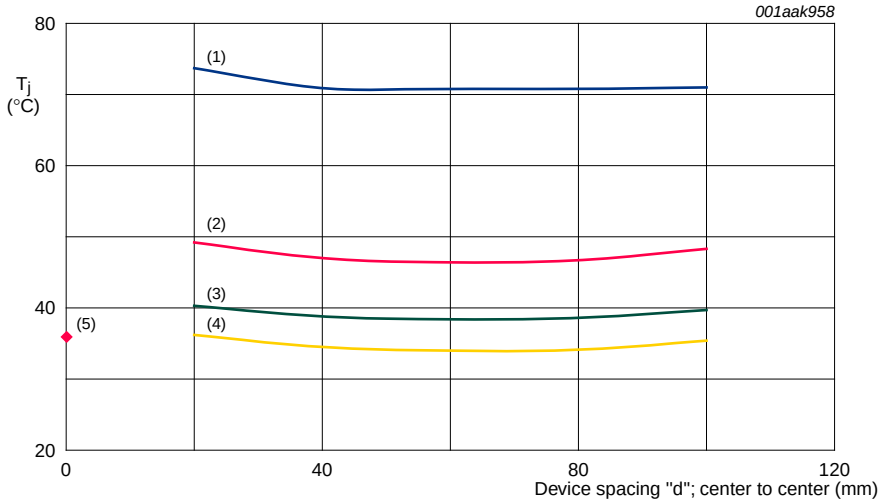
Figure 18 demonstrates two possible circuit configurations for two MOSFETs with independently connected drains. Figure 18(a) shows two high-side load switches connected to different supply (V_{BAT}) lines – a common automotive configuration. Figure 18(b) we have the two MOSFETs connected in a half-bridge configuration typical of a unidirectional motor drive controller or DC-DC buck converter circuit. In both cases, the MOSFET drains do not share a common electrical connection. The modified layer stack-up corresponding to these topologies is shown in Figure 19.



(1) Layer 1 (power).
(2) Layer 2 (ground).
(3) Layer 3 (signal).
(4) Layer 4 (power and signal).

Fig 19. Modified 4-layer stack-up (not to scale)

The stack-up of Figure 19 shows the ground plane on layer 2 with the device drain connected to areas on both layer 1 and layer 4, and with the layer 4 copper now also a square of dimensions 15 mm × 15 mm. Layer 3 remains a signal layer. Both MOSFETs are configured in this way, and once again we investigate the influence of separation distance “d” on device T_j. The results are shown in Figure 20, together with those for the previous analyses.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, separate drains.

(5) Half-bridge configuration.

Fig 20. Simulation results for two devices of varying separation “d” on a 4-layer PCB with vias

Clearly the addition of vias under the devices results in a further decrease in T_j even though the layer 4 copper area is reduced. Once again we see that T_j has little dependence on device spacing.

Also shown in Figure 20 is the result for the two devices positioned in a “half-bridge configuration”. This refers to the circuit topology of see Figure 18(b), where it makes sense from an electrical point of view to position the devices one above the other rather than side by side. In this way, the source connection of Q1 is physically close to the drain connection of Q2 and connection between the two would be by a short, low inductance path. See Figure 21.

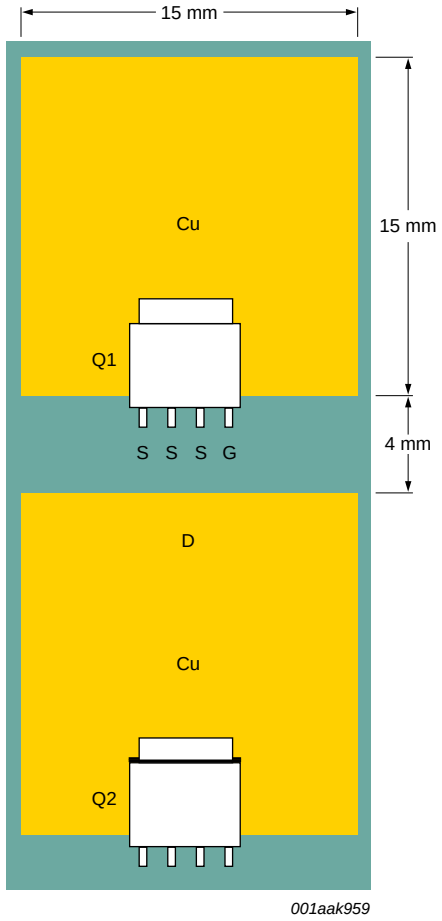
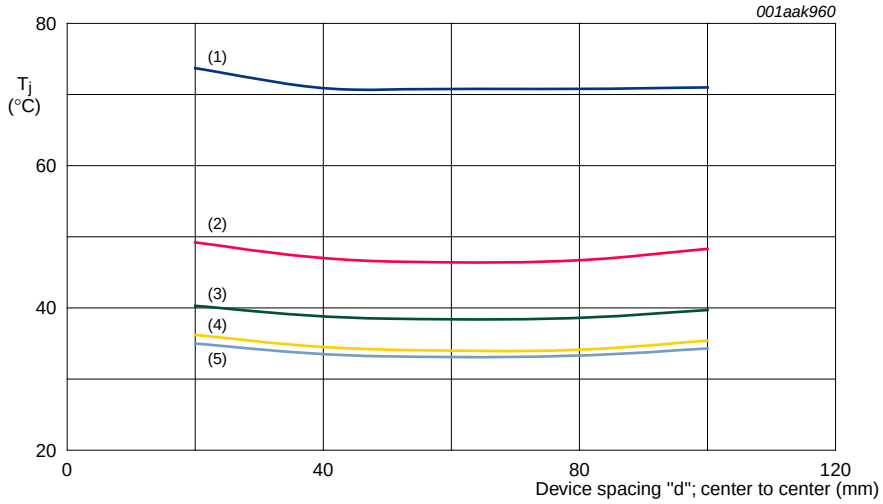


Fig 21. Two devices logically positioned for a half-bridge configuration

4.5 Analysis 8: A 4-layer PCB with thermal vias part 2

The second analysis will consider two devices sharing a common drain connection. This would correspond to the topology of Figure 18(a) with a common V_{BAT} line. The V_{BAT} line is represented by a plane measuring 25 mm × 120 mm on layer 4, with vias as per the previous analysis. Results are shown in Figure 22.



(1) Layer 1 only.
(2) 2-layer.
(3) 4-layer.
(4) 4-layer with vias, separate drains.
(5) 4-layer with vias and common V_{BAT} plane.

Fig 22. Simulation results for two devices of varying separation “d” on a 4-layer PCB with vias and common V_{BAT} plane

The improvement in thermal performance is practically negligible compared to the previous example (Section 4.4) with independent drain copper areas.

4.6 Summary: factors affecting the thermal performance of two devices

To reiterate, the following results were obtained with layer 1 copper side lengths of 15 mm.

- For two devices mounted on a single-layer PCB, device T_j is largely independent of device spacing “d”. A significant increase in T_j vis only observed when the devices are mounted very close together. There is also little difference compared to the single device case (see Figure 15). Device T_j is approximately 71 °C
- Adding a second copper layer (layer 4) reduces T_j by roughly 20 °C to 25 °C compared to the single-layer case. Some minor dependence of T_j on “d” is apparent, with slightly higher T_j occurring when the devices are mounted closest together or at the PCB edges (see Figure 16)
- Moving to a 4-layer PCB stack-up yields a further reduction in T_j of ~9 °C compared to the 2-layer design (see Figure 17)
- Adding a 4 × 4 pattern of vias under the devices provides a further small improvement in thermal performance, whereby T_j is reduced by an additional ~4 °C (see pcb)
- Making the device layer 4 copper areas common, rather than separate, has almost no effect on device T_j (see Figure 22)

5. Four LFPAK devices

In this final section the number of devices will be increased to four. We will adopt the same PCB size as for the analyses in Section 4 on page 19, and a similar approach in building up the PCB stack-up from a simple structure to one which is more complex. As before, in order to restrict the number of variables to a sensible limit we will consider only the 15 mm side-length area for layer 1. This section will mainly concentrate on the four devices equally spaced apart in a single line (see Figure 23), but will also consider two of the “half bridge” configurations described in Section 4.3 on page 22.

The PCB top copper configuration is shown in Figure 23.

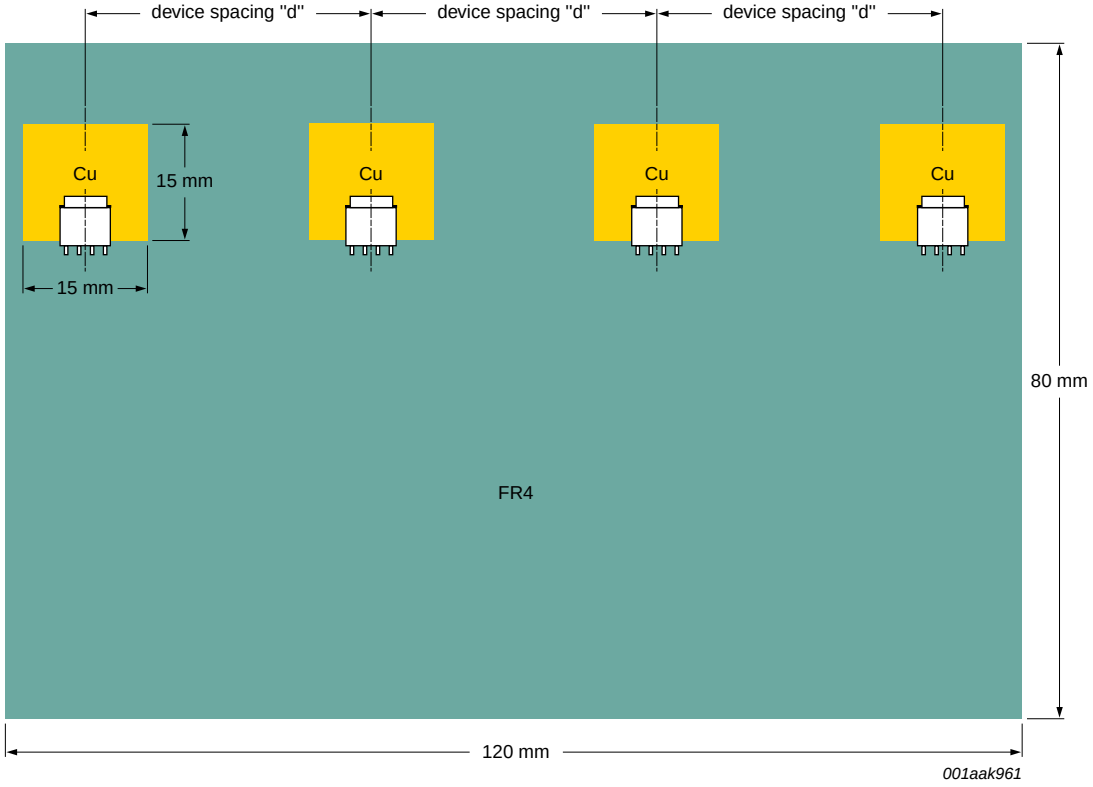


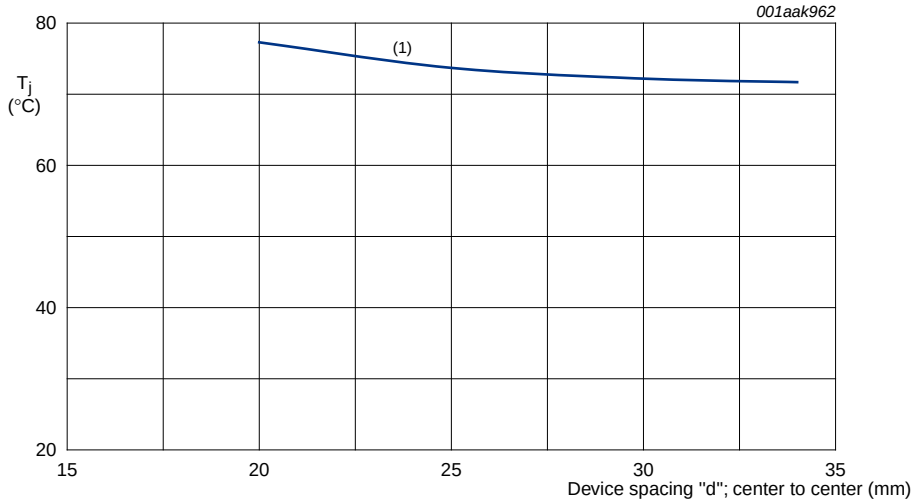
Fig 23. Four devices: PCB top copper configuration

Simulation were carried out to investigate the influence of “d” on device T_j for the various PCB stack-ups. Values of d varied from 34 mm (maximum separation, as shown in Figure 23) to 20 mm where there was only a 5 mm gap between the device layer 1 copper areas.

5.1 Analysis 9: A single-layer PCB

The results for the single-layer simulations are shown in Figure 24. Unlike the analyses of two devices in the previous section, the thermal environment is not exactly the same for all four devices in this configuration. The two inner devices are at a slight disadvantage as they have additional heat sources on both their left- and right-hand sides, whilst the outer devices have a heat source on one side only. In the worst case, this results in a difference

in T_j value of approximately 3 °C between inner and outer devices. In the interests of presenting a conservative set of results, the graphs which follow show the temperatures for the inner, slightly hotter, devices.



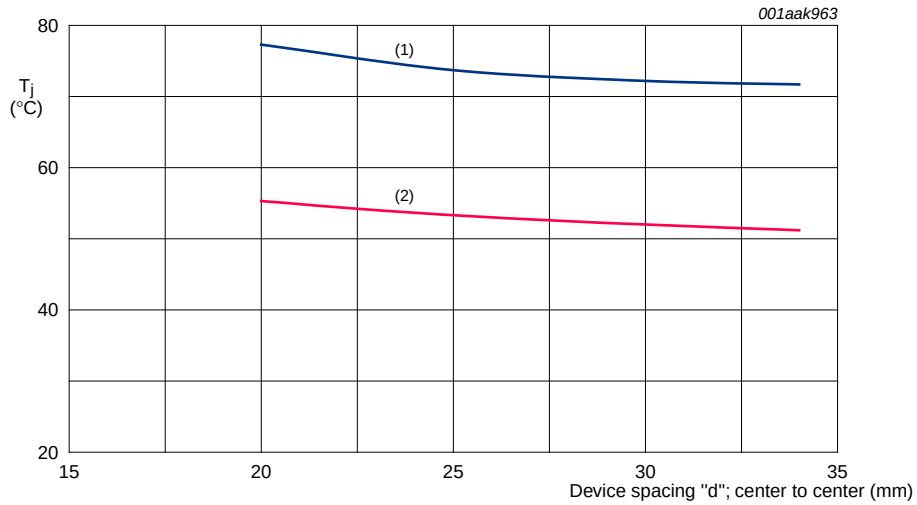
(1) Layer 1 only.

Fig 24. Simulation results for four devices of varying separation “d” on a single-layer PCB

Again, we see the law of diminishing returns exhibited in these results: as the spacing between devices increases, so the curves flattens out. Therefore, increasing the centre – center spacing beyond approximately 30 mm would have little influence on device temperatures.

5.2 Analysis 10: A 2-layer PCB

For the purposes of this exercise we will again consider the same variations in device spacing as for analysis 9. However for analysis 10 we will add the layer 4 (bottom copper) layer covering the whole of the underside of the PCB and thereby creating a 2-layer stack-up. In practical terms this layer might be a ground or power plane, although it remains unconnected to the devices. The results are shown in the graph of Figure 25 together with those from analysis 9 for comparison purposes.



(1) Layer 1 only.

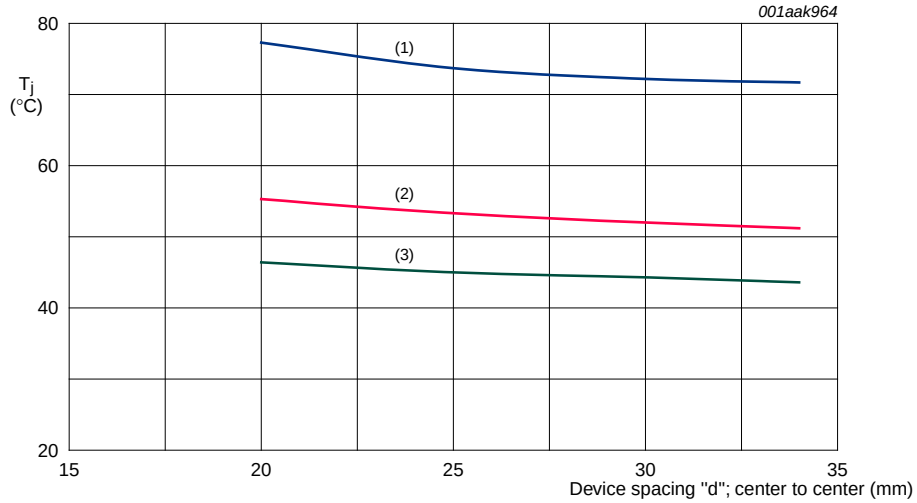
(2) 2-layer.

Fig 25. Simulation results for four devices of varying separation “d” on a 2-layer PCB

Adding the second copper layer increases the thermal conductivity of the PCB and reduces device temperatures by approximately 20 °C. This is exactly the result we would expect and is in keeping with the results for the one and two-device configurations.

5.3 Analysis 11: A generalized 4-layer PCB

The 2-layer stack-up of analysis 10 will now be increased to 4 layers with the addition of two internal signal layers. The signal layers are assumed to be composed of numerous thin signal tracks, and simulation of the internal layers will again be by the “percentage coverage” method, 50 % copper coverage and 1 oz./ft^2 (35 μm) thickness. Layer 4 remains a solid unconnected plane covering the entire underside area. See Figure 8. Junction temperatures were determined for various separation distances d and the results are shown in Figure 26.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

Fig 26. Simulation results for four devices of varying separation “d” on a 4-layer PCB

Adding the internal signal layers has resulted in an overall reduction in T_j of approximately 8 °C.

5.4 Analysis 12: A 4-layer PCB with thermal vias part 1

In analysis 12 we will consider cases where the layer 1 copper areas (connected to MOSFET drains) are connected to 15 mm × 15 mm copper areas on layer 4 by thermal/electrical vias of the 5 × 4 pattern described in Section 3.5 on page 16. The corresponding circuit topologies are as shown in Figure 18, but for twice the number of devices. We could therefore have four high-side load switches connected to four different V_{BAT} lines (Figure 18(a)). Alternatively we could have two of the half-bridge topologies shown in Figure 18(b). For either possibility, each MOSFET’s drain connections are independent, and layer 2 in the PCB stack-up is a full-coverage ground plane (see Figure 19).

For the four high-side load switches we will vary the spacing between devices as in analyses 9 to 11. In the case of the two half-bridges, however, we can consider each half-bridge as a single “unit”, and examine the effect of varying the spacing between half-bridge units. See Figure 27). The results are shown in Figure 28.

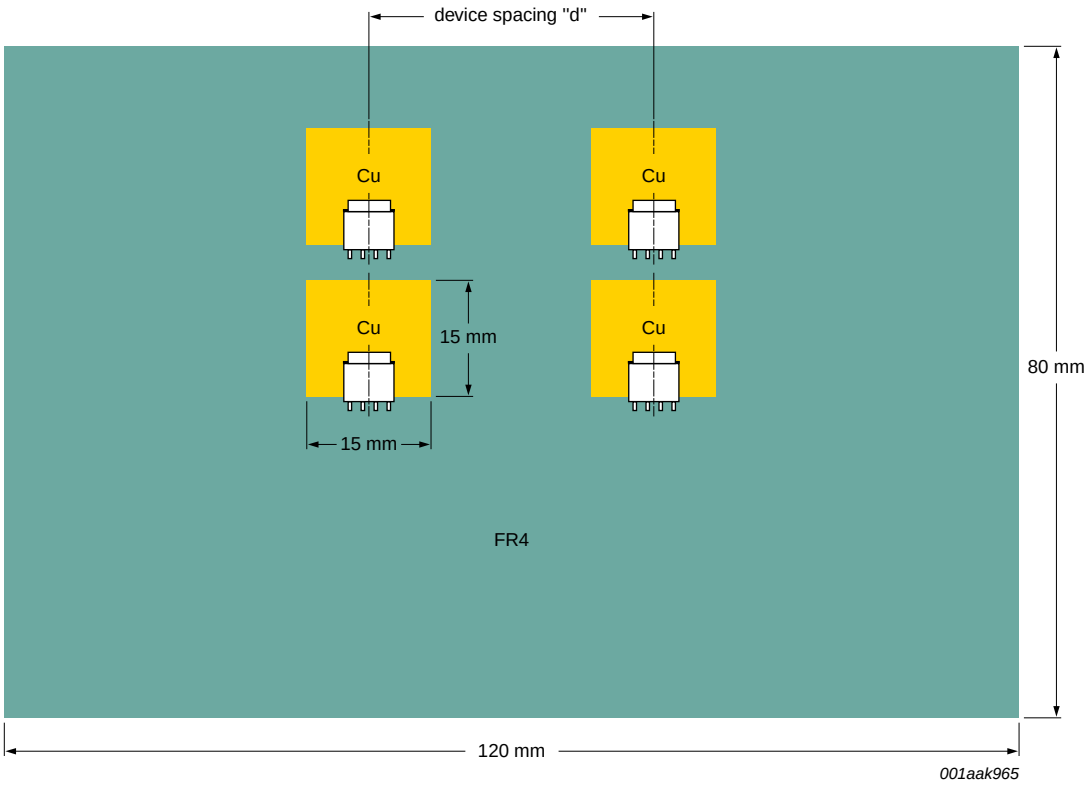
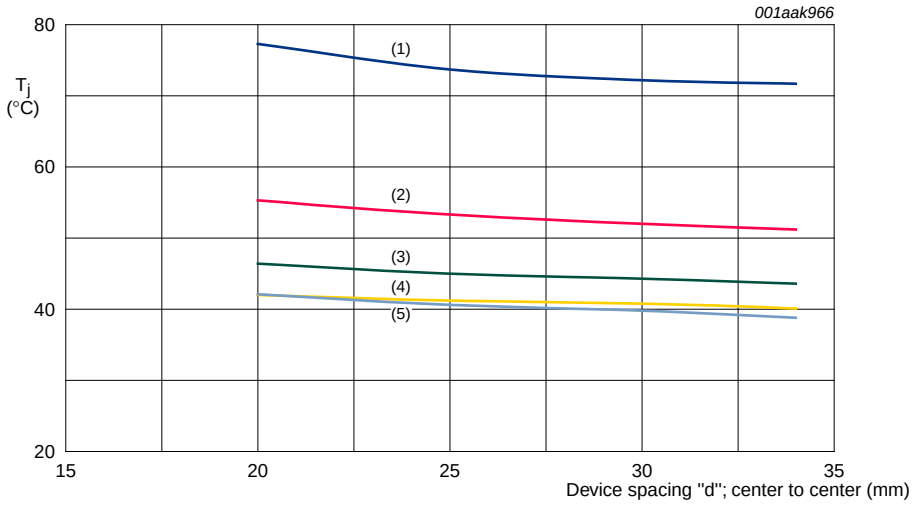


Fig 27. Four devices positioned as two half-bridges configurations



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, half-bridge configuration.

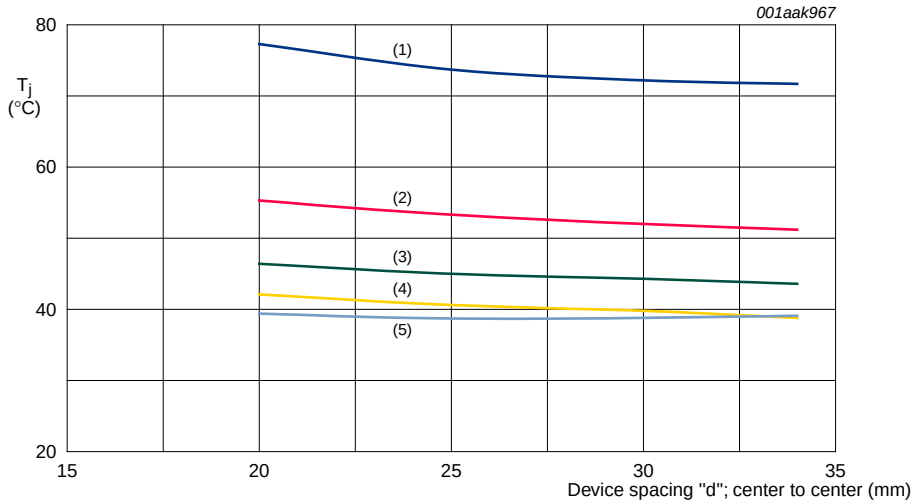
(5) 4-layer with vias, separate drains.

Fig 28. Simulation results for four devices of varying separation “d” on a 4-layer PCB with vias

Adding vias under the devices results in an overall reduction in T_j of approximately 4 °C to 5 °C for both topologies.

5.5 Analysis 12: A 4-layer PCB with thermal vias part 2

The final analysis will consider four devices sharing a common drain connection. This would correspond to the topology of Figure 18(a) with a common V_{BAT} line. The V_{BAT} line is represented by a plane measuring 25 mm × 120 mm on layer 4, and stack-up is as Figure 19. The results are shown in Figure 29.



(1) Layer 1 only.

(2) 2-layer.

(3) 4-layer.

(4) 4-layer with vias, separate drains.

(5) 4-layer with vias and common V_{BAT} plane.

Fig 29. Simulation results for four devices of varying separation “d” on a 4-layer PCB with vias and common V_{BAT} plane

Connecting the four devices does make a small difference to T_j when the devices are close together, however as “d” increases the effect tends to diminish.

5.6 Summary; factors affecting the thermal performance of four devices

For layer 1 copper side lengths of 15 mm.

- For four devices mounted on a single-layer PCB, device T_j is somewhat independent of device spacing “d”. The inner two devices tend to run slightly hotter, by approximately 3 °C in the worst case. Device T_j is approximately 72 °C (see Figure 24)
- Adding a second copper layer (layer 4) reduces T_j by roughly 20 °C compared to the single-layer case (see Figure 25)
- Moving to a 4-layer PCB stack-up yields a further reduction in T_j of ~8 °C compared to the 2-layer design (see Figure 26)
- Adding a 4 × 4 pattern of vias under the devices provides a further small improvement in thermal performance, whereby T_j is reduced by an additional ~4 °C (see Figure 28)
- Making the device layer 4 copper areas common, rather than separate, has little effect on device (see Figure 29)

6. Summary

Increasingly there is a need to pay attention to the thermal aspects of PCB design, in order that safe operating temperatures are not exceeded. For designs employing surface-mount power MOSFETs, which use the PCB as their primary method of heatsinking, it is important that both MOSFET junction temperature (T_j) and PCB temperature (T_{PCB}) are kept within safe limits. Typically the maximum permissible T_j figure is 175 °C whilst the maximum T_{PCB} figure may be 120 °C. As there is close thermal coupling between the MOSFET device and the PCB to which it is soldered we can say that $T_{PCB} \approx T_j$ and so the operating temperature upper limit is that of the PCB (120 °C) rather than the MOSFET junction.

The PCB designer may be faced with a lack of useful resources when attempting to lay out a PCB for “safe” thermal operation. At one extreme, the MOSFET data sheet R_{th} figures are too vague to be of use and will probably have been measured under conditions which differ greatly from those of his target application. At the other extreme, a detailed analysis of the thermal performance of a design may be carried out using simulation software and/or actual prototype build. Simulation software can give excellent results in a relatively short space of time, but is generally expensive and its use has a steep learning curve. Prototype build, on the other hand, will almost certainly be required at some stage in the product development, for design verification, but is an expensive and time-consuming option in the early stages of the design cycle. There is therefore a need for thermal design guidelines, which bridge the gulf between the less-than-helpful R_{th} figures at one extreme and full prototype simulation or build at the other, and which may be employed at an early stage in the PCB design in order to steer the designer in the right direction. The purpose of this document is to provide those guidelines for designs employing the NXP Semiconductors range of LFPAK MOSFETs

This design guide has considered the thermal performance of a variety of different PCB configurations and stack-ups for one, two and four MOSFET devices. Factors which have been considered include; PCB layer stack-up, the influence of common circuit topologies on PCB layout, PCB copper area, the influence of thermal “vias”, device placement and spacing and the implications of multiple dissipating devices on a single PCB. This

document cannot hope to address all the myriad possible device usages, however it is hoped that the chosen range of different configurations is representative of typical “real life” device usage.

Finally, we should reiterate again that the information contained within this design guide is presented as a starting point only. Any new design should of course be prototyped and its thermal behavior characterized before placing the design into production.

7. Abbreviations

Table 2. Abbreviations

Acronym	Description
EMC	ElectroMagnetic Compatibility
LFPAK	Loss-Free Package
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed-Circuit Board
SMD	Surface-Mounted Device

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